

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A local module and a plurality of remote modules, each of the local module and plurality of remote modules including a coherence controller capable of being connected to a plurality of multiprocessors within the same module, each of the multiprocessors including a local main memory and a plurality of processors each equipped with a cache memory, each coherence controller comprising:

a cache filter directory including a first filter directory for guaranteeing coherence between the local main memory and the cache memory within each respective coherence controller;

a complementary filter directory for tracking locations of lines or blocks of the local main memory of the local module copied from the local module into at least one remote module and for guaranteeing coherence between the local main memory and the cache memory of the local module and said at least one remote module; and

an external port connected to said at least one remote module.

2. (Currently Amended) A coherence controller according to claim 1, wherein ~~the~~ each respective cache filter directory includes:

an “n”-bit presence vector where n is a number of multiprocessors in the ~~local~~ module,

an $[[n-1]]N-1$ -bit extension of the presence vector, where $[[n-1]]N-1$ is a total number of remote modules connected to the external port, and
an Exclusive status bit.

3. (Previously Presented) A coherence controller according to claim 2, wherein the external port is connected directly or indirectly to said at least one remote module via an external two-point link.

4. (Previously Presented) A coherence controller according to claim 2, further comprising:

"n" control units connected to the n multiprocessors in the local module,
a control unit XPU connected to the external port, and
a common control unit containing the cache filter directory.

5. (Previously Presented) A coherence controller according to claim 4, wherein the control unit XPU and the "n" control units are compatible with one another and use at least substantially similar protocols.

6. (Previously Presented) A multiprocessor module connected to a coherence controller as recited in claim 1.

7. (Previously Presented) A multiprocessor system with a multimodule architecture, comprising:

at least two multiprocessor modules as recited in claim 6, connected to one another directly or indirectly through external ports of coherence controllers located within said at least two multiprocessor modules.

8. (Previously Presented) A multiprocessor system according to claim 7, wherein said external ports are connected to one another through a switching device or router.

9. (Previously Presented) A multiprocessor system according to claim 8, wherein the switching device or router includes a unit which manages and/or filters data and/or requests in transit between said at least two multiprocessor modules.

10. (Currently Amended) A large-scale symmetric multiprocessor server with a multimodule architecture, comprising:

a plurality of multiprocessor modules including a local multiprocessor module and a remote multiprocessor module, each of said multiprocessor modules including:

a plurality of multiprocessors each equipped with at least one cache memory and at least one local main memory, and

a local coherence controller connected to said multiprocessors within the same module and including a local cache filter directory for guaranteeing local coherence between the local main memory and the cache memories ~~in each of said multiprocessors~~ within the same module, said local coherence controller connected to at least said remote multiprocessor module,

wherein the local coherence controller further includes:

a complementary cache filter directory for tracking a location of memory lines or blocks copied from said ~~first~~ local multiprocessor module to ~~the second one of said multiprocessor modules~~ said remote multiprocessor module and for guaranteeing coherence between the local main memory and the cache memories ~~in each of the multiprocessors in said first~~ local processor module and said remote multiprocessor module.

11. (Currently Amended) A multiprocessor server with a multimodule architecture according to claim 10, wherein the coherence controller includes:

an “n”-bit presence vector which indicates presence or absence of a copy of a memory block or line in the cache memories of the multiprocessors,

an [[“n-1”]] “N-1”-bit extension of the presence vector which indicates presence or absence of a copy of a memory block or line in cache memories of multiprocessors in said remote multiprocessor module, and

an Exclusive status bit.

12. (Previously Presented) A multiprocessor server with a multimodule architecture according to claim 10, further comprising:

a switching device or router which connects the first multiprocessor module with said remote multiprocessor module, said switching device or router including a unit which manages and/or filters data and/or requests in transit between the first multiprocessor module and the said remote multiprocessor module.